

TLP352

1. Applications

- Transistor Inverters
- MOSFET Gate Drivers
- IGBT Gate Drivers
- Induction Cooktop and Home Appliances

2. General

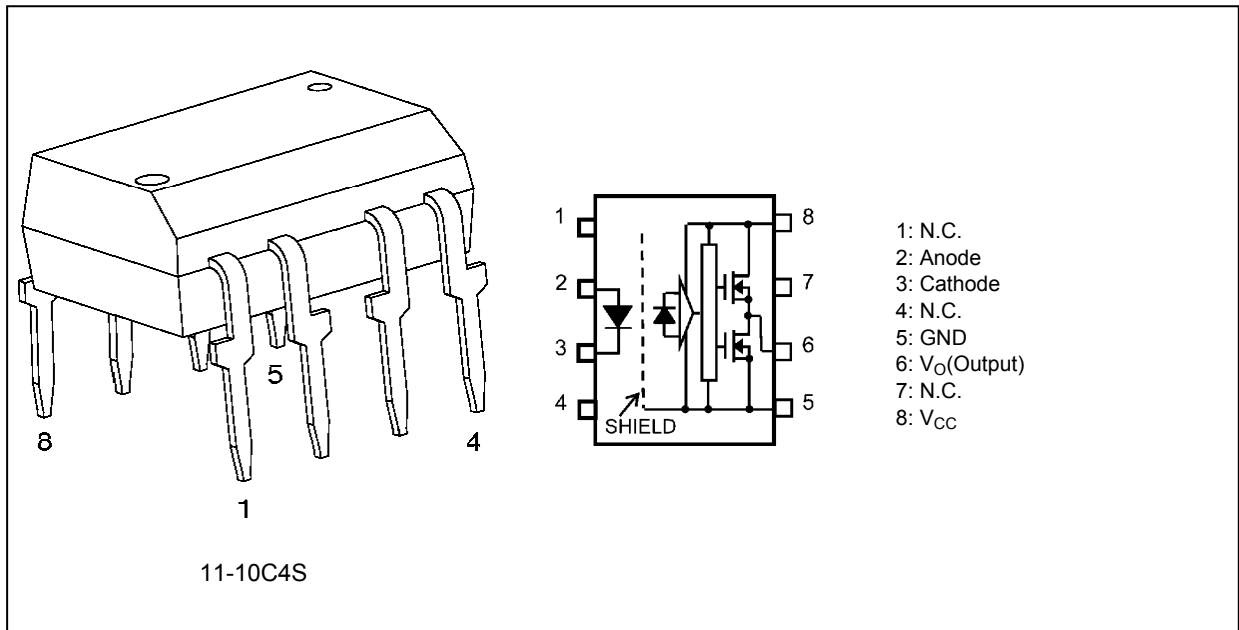
The TLP352 is a photocoupler in a DIP8 package that consists of a GaAs infrared light-emitting diode (LED) optically coupled to an integrated high-gain, high-speed photodetector IC chip. It provides guaranteed performance and specifications at temperatures up to 125°C.

The TLP352 has an internal Faraday shield that provides a guaranteed Common-mode transient immunity of 20 kV/μs. It has a totem-pole output that can both sink and source current. The TLP352 is ideal for IGBT and power MOSFET gate drive.

3. Features

- (1) Buffer logic type (totem pole output)
 - (2) Output peak current: ±2.5 A (max)
 - (3) Operating temperature: -40 to 125°C
 - (4) Supply current: 3 mA (max)
 - (5) Supply voltage: 15 to 30 V
 - (6) Threshold input current: 5 mA (max)
 - (7) Propagation delay time: $t_{pHL}/t_{pLH} = 200$ ns (max)
 - (8) Common-mode transient immunity: ±20 kV/μs (min)
 - (9) Isolation voltage: 3750 Vrms (min)
 - (10) Safety standards
 - UL-approved: UL1577 File No.E67349
 - cUL-approved: CSA Component Acceptance Service No.5A, File No.E67349
 - VDE-approved: Option (D4) EN60747-5-5(Note)
- (Note): When an EN60747-5-5 approved type is needed, please designate the Option (D4).

4. Packaging and Pin Configuration



5. Internal Circuit (Note)

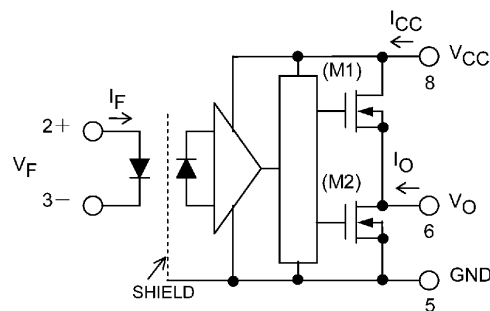


Fig. 5.1 Internal Circuit

Note: A 0.1- μ F bypass capacitor must be connected between pin 8 and pin 5.

6. Principle of Operation

6.1. Truth Table

| Input | LED | M1 | M2 | Output |
|-------|-----|-----|-----|--------|
| H | ON | ON | OFF | H |
| L | OFF | OFF | ON | L |

6.2. Mechanical Parameters

| Characteristics | 7.62-mm Pitch TLP352 | 10.16-mm Pitch TLP352F | Unit |
|------------------------------|-------------------------|---------------------------|------|
| Creepage distances | 7.0 (min) | 8.0 (min) | mm |
| Clearance distances | 7.0 (min) | 8.0 (min) | |
| Internal isolation thickness | 0.4 (min) | 0.4 (min) | |

7. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25°C)

| | Characteristics | Symbol | Note | Rating | Unit |
|----------|--|------------------------------------|----------|------------|-------|
| LED | Input forward current | I _F | | 20 | mA |
| | Input forward current derating (T _a ≥ 116°C) | ΔI _F /ΔT _a | | -0.6 | mA/°C |
| | Peak transient input forward current | I _{FPT} | (Note 1) | 1 | A |
| | Peak transient input forward current derating (T _a ≥ 110°C) | ΔI _{FPT} /ΔT _a | | -25 | mA/°C |
| | Input reverse voltage | V _R | | 5 | V |
| | Input power dissipation | P _D | | 40 | mW |
| | Input power dissipation derating (T _a ≥ 110°C) | ΔP _D /ΔT _a | | -1.0 | mW/°C |
| Detector | Peak high-level output current (T _a = -40 to 125°C) | I _{OPH} | (Note 2) | -2.5 | A |
| | Peak low-level output current (T _a = -40 to 125°C) | I _{OPL} | (Note 2) | +2.5 | |
| | Output voltage | V _O | | 35 | V |
| | Supply voltage | V _{CC} | | 35 | |
| | Output power dissipation | P _O | | 260 | mW |
| | Output power dissipation derating (T _a ≥ 110°C) | ΔP _O /ΔT _a | | -6.5 | mW/°C |
| Common | Operating temperature | T _{opr} | | -40 to 125 | °C |
| | Storage temperature | T _{stg} | | -55 to 150 | |
| | Lead soldering temperature (10 s) | T _{sol} | (Note 3) | 260 | |
| | Isolation voltage AC, 60 s, R.H. ≤ 60%, T _a = 25°C | BV _S | (Note 4) | 3750 | Vrms |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width (PW) ≤ 1 μs, 300 pps

Note 2: Exponential waveform. Pulse width ≤ 0.3 μs, f ≤ 15 kHz

Note 3: ≥ 2 mm below seating plane.

Note 4: This device is considered as a two-terminal device: Pins 1, 2, 3 and 4 are shorted together, and pins 5, 6, 7 and 8 are shorted together.

8. Recommended Operating Conditions (Note)

| Characteristics | Symbol | Note | Min | Typ. | Max | Unit |
|--------------------------------|--------------|----------|-----|------|------|------|
| Input on-state current | $I_{F(ON)}$ | (Note 1) | 6.5 | — | 10 | mA |
| Input off-state voltage | $V_{F(OFF)}$ | | 0 | — | 0.8 | V |
| Supply voltage | V_{CC} | (Note 2) | 15 | — | 30 | |
| Peak high-level output current | I_{OPH} | | — | — | -2.0 | A |
| Peak low-level output current | I_{OPL} | | — | — | +2.0 | |
| Operating frequency | f | (Note 3) | — | — | 50 | kHz |

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this datasheet should also be considered.

Note: A ceramic capacitor (0.1 μ F) should be connected between pin 8 and pin 5 to stabilize the operation of a high-gain linear amplifier. Otherwise, this photocoupler may not switch properly. The bypass capacitor should be placed within 1 cm of each pin.

Note: If the rising slope of the supply voltage(V_{CC}) for the detector is steep, stable operation of the internal circuits cannot be guaranteed.

Be sure to set 3.0 V/ μ s or less for a rising slope of the V_{CC} .

Note 1: The rise and fall times of the input on-current should be less than 0.5 μ s.

Note 2: Denotes the operating range, not the recommended operating condition.

Note 3: Exponential waveform. $I_{OPH} \geq -2.0$ A (≤ 0.3 μ s), $I_{OPL} \leq 2.0$ A (≤ 0.3 μ s), $T_a = 125^\circ$ C

9. Electrical Characteristics (Note)(Unless otherwise specified, $T_a = -40$ to 125° C)

| Characteristics | Symbol | Note | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|---------------------------|----------|--------------|--|------|-------|-------|----------------|
| Input forward voltage | V_F | | | $I_F = 10$ mA, $T_a = 25^\circ$ C | 1.4 | 1.55 | 1.7 | V |
| Input forward voltage temperature coefficient | $\Delta V_F / \Delta T_a$ | | | $I_F = 10$ mA | — | -2.0 | — | mV/ $^\circ$ C |
| Input reverse current | I_R | | | $V_R = 5$ V, $T_a = 25^\circ$ C | — | — | 10 | μ A |
| Input capacitance | C_t | | | $V = 0$ V, $f = 1$ MHz, $T_a = 25^\circ$ C | — | 95 | — | pF |
| Peak high-level output current | I_{OPH} | (Note 1) | Fig. 12.1.1 | $I_F = 5$ mA, $V_{CC} = 30$ V, $V_{8-6} = -3.5$ V | — | -1.6 | -1.0 | A |
| | | | | $I_F = 5$ mA, $V_{CC} = 15$ V, $V_{8-6} = -7.0$ V | — | — | -2.0 | |
| Peak low-level output current | I_{OPL} | (Note 1) | Fig. 12.1.2 | $I_F = 0$ mA, $V_{CC} = 30$ V, $V_{6-5} = 2.5$ V | 1.0 | 1.6 | — | |
| | | | | $I_F = 0$ mA, $V_{CC} = 15$ V, $V_{6-5} = 7.0$ V | 2.0 | — | — | |
| High-level output voltage | V_{OH} | | Fig. 12.1.3 | $I_F = 5$ mA, $R_L = 200$ Ω , $V_{CC1} = +15$ V, $V_{EE1} = -15$ V | 11.0 | 13.7 | — | V |
| Low-level output voltage | V_{OL} | | Fig. 12.1.4 | $V_F = 0.8$ V, $R_L = 200$ Ω , $V_{CC1} = +15$ V, $V_{EE1} = -15$ V | — | -14.9 | -12.5 | |
| High-level supply current | I_{CCH} | | Fig. 12.1.5 | $I_F = 10$ mA, $V_{CC} = 30$ V, $V_O = \text{Open}$ | — | 1.5 | 3.0 | mA |
| Low-level supply current | I_{CCL} | | Fig. 12.1.6 | $I_F = 0$ mA, $V_{CC} = 30$ V, $V_O = \text{Open}$ | — | 1.5 | 3.0 | |
| Threshold input current (L/H) | I_{FLH} | | | $V_{CC} = 15$ V, $V_O > 1$ V | — | 1.0 | 5 | |
| Threshold input voltage (H/L) | V_{FHL} | | | $V_{CC} = 15$ V, $V_O < 1$ V | 0.8 | — | — | V |
| Supply voltage | V_{CC} | | | — | 15 | — | 30 | |
| UVLO threshold voltage | V_{UVLO+} | | | $I_F = 5$ mA, $V_O > 2.5$ V | 11.0 | 12.5 | 13.5 | |
| | V_{UVLO-} | | | $I_F = 5$ mA, $V_O < 2.5$ V | 9.5 | 11.0 | 12.0 | |
| UVLO hysteresis | $UVLO_{HYS}$ | | | — | — | 1.5 | — | |

Note: All typical values are at $T_a = 25^\circ$ C.

Note: This device is designed for low power consumption, making it more sensitive to ESD than its predecessors. Extra care should be taken in the design of circuitry and pc board implementation to avoid ESD problems.

Note 1: I_O application time ≤ 50 μ s, single pulse.

10. Isolation Characteristics (Unless otherwise specified, $T_a = 25^\circ\text{C}$)

| Characteristics | Symbol | Note | Test Conditions | Min | Typ. | Max | Unit |
|-------------------------------------|--------|----------|---|--------------------|-----------|-----|----------|
| Total capacitance (input to output) | C_S | (Note 1) | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ | — | 1.0 | — | pF |
| Isolation resistance | R_S | (Note 1) | $V_S = 500\text{ V}$, R.H. $\leq 60\%$ | 1×10^{12} | 10^{14} | — | Ω |
| Isolation voltage | BV_S | (Note 1) | AC, 60 s | 3750 | — | — | Vrms |
| | | | AC, 1 s, in oil | — | 10000 | — | |
| | | | DC, 60 s, in oil | — | 10000 | — | Vdc |

Note 1: This device is considered as a two-terminal device: Pins 1, 2, 3 and 4 are shorted together, and pins 5, 6, 7 and 8 are shorted together.

11. Switching Characteristics (Note)(Unless otherwise specified, $T_a = -40$ to 125°C)

| Characteristics | Symbol | Note | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---|-----------------------|----------------------|--------------|---|----------|----------|-----|-------------------|
| Propagation delay time (L/H) | t_{pLH} | (Note 1) | Fig. 12.1.7 | $I_F = 0 \rightarrow 5\text{ mA}$, $V_{CC} = 30\text{ V}$, $R_g = 20\ \Omega$, $C_g = 10\text{ nF}$ | 50 | 130 | 200 | ns |
| Propagation delay time (H/L) | t_{pHL} | (Note 1) | | $I_F = 5 \rightarrow 0\text{ mA}$, $V_{CC} = 30\text{ V}$, $R_g = 20\ \Omega$, $C_g = 10\text{ nF}$ | 50 | 130 | 200 | |
| Pulse width distortion | $ t_{pHL} - t_{pLH} $ | (Note 1) | | $I_F = 0 \leftrightarrow 5\text{ mA}$, $V_{CC} = 30\text{ V}$, $R_g = 20\ \Omega$, $C_g = 10\text{ nF}$ | — | — | 50 | |
| Propagation delay skew (device to device) | t_{psk} | (Note 1) (Note 4) | | $I_F = 0 \leftrightarrow 5\text{ mA}$, $V_{CC} = 30\text{ V}$, $R_g = 20\ \Omega$, $C_g = 10\text{ nF}$ | -80 | — | 80 | |
| Rise time | t_r | (Note 1) | | $I_F = 0 \rightarrow 5\text{ mA}$, $V_{CC} = 30\text{ V}$, $R_g = 20\ \Omega$, $C_g = 10\text{ nF}$ | — | 15 | — | |
| Fall time | t_f | (Note 1) | | $I_F = 5 \rightarrow 0\text{ mA}$, $V_{CC} = 30\text{ V}$, $R_g = 20\ \Omega$, $C_g = 10\text{ nF}$ | — | 8 | — | |
| Common-mode transient immunity at output high | CM_H | (Note 2) | Fig. 12.1.8 | $V_{CM} = 1000\text{ V}_{p-p}$, $I_F = 5\text{ mA}$, $V_{CC} = 30\text{ V}$, $T_a = 25^\circ\text{C}$, $V_{O(min)} = 26\text{ V}$ | ± 20 | ± 25 | — | kV/ μs |
| Common-mode transient immunity at output low | CM_L | (Note 3) | | $V_{CM} = 1000\text{ V}_{p-p}$, $I_F = 0\text{ mA}$, $V_{CC} = 30\text{ V}$, $T_a = 25^\circ\text{C}$, $V_{O(max)} = 1\text{ V}$ | ± 20 | ± 25 | — | |

Note: All typical values are at $T_a = 25^\circ\text{C}$.

Note 1: Input signal ($f = 25\text{ kHz}$, duty = 50%, $t_r = t_f = 5\text{ ns}$ or less).

C_L is approximately 15 pF which includes probe and stray wiring capacitance.

Note 2: CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 26\text{ V}$).

Note 3: CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 1\text{ V}$).

Note 4: The propagation delay skew, t_{psk} , is equal to the magnitude of the worst-case difference in t_{pHL} and/or t_{pLH} that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).

12. Test Circuits and Characteristics Curves

12.1. Test Circuits

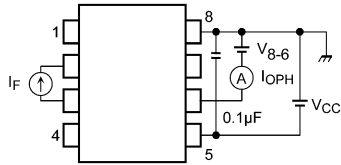


Fig. 12.1.1 I_{OPH} Test Circuit

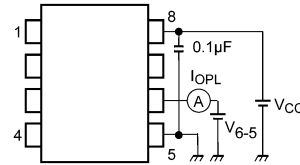


Fig. 12.1.2 I_{OPL} Test Circuit

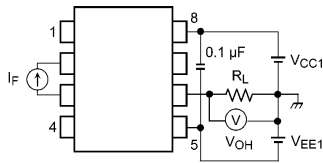


Fig. 12.1.3 V_{OH} Test Circuit

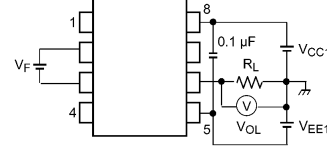


Fig. 12.1.4 V_{OL} Test Circuit

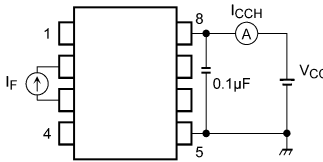


Fig. 12.1.5 I_{CCH} Test Circuit

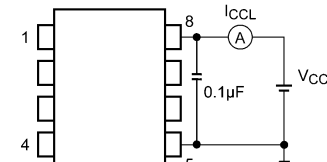
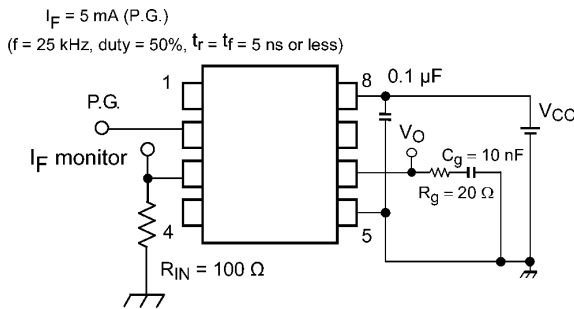
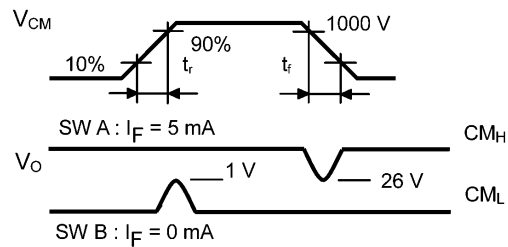
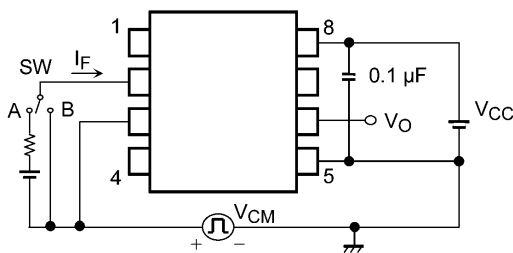
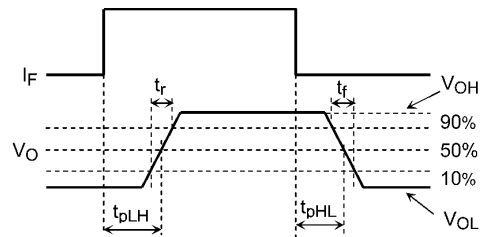


Fig. 12.1.6 I_{CCL} Test Circuit



P.G.: Pulse generator

Fig. 12.1.7 Switching Time Test Circuit



$$CM_L = \frac{800(V)}{t_r(\mu s)} \quad CM_H = -\frac{800(V)}{t_f(\mu s)}$$

CM_L (CM_H) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

Fig. 12.1.8 Common-Mode Transient Immunity

12.2. Characteristics Curves (Note)

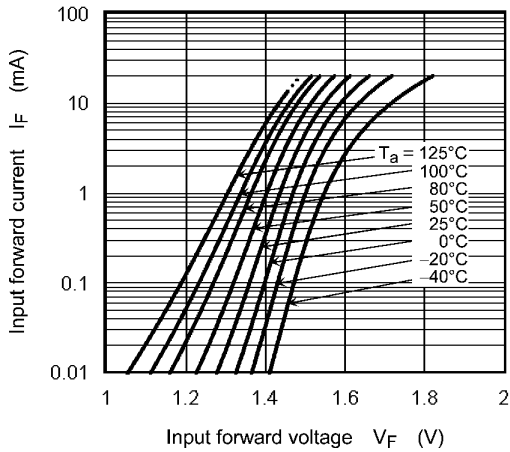


Fig. 12.2.1 $I_F - V_F$

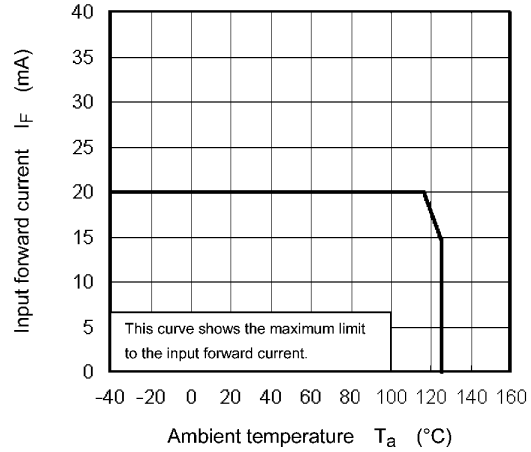


Fig. 12.2.2 $I_F - T_a$

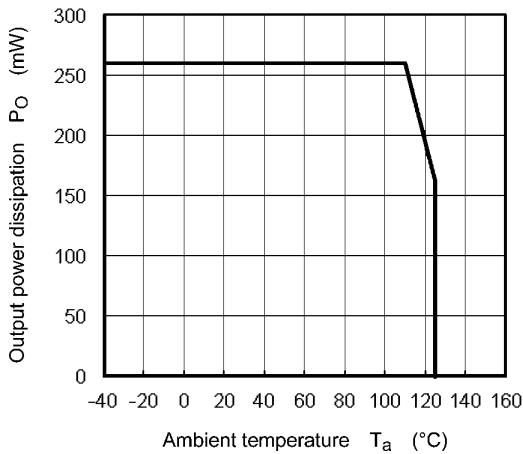


Fig. 12.2.3 $P_O - T_a$

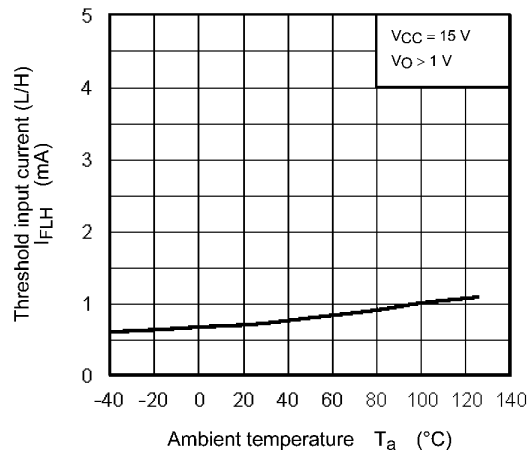


Fig. 12.2.4 $I_{FLH} - T_a$

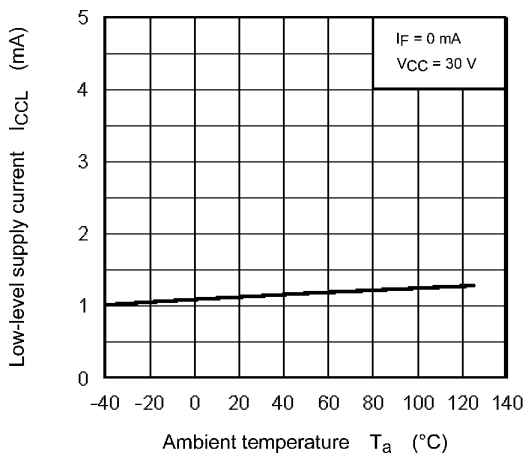


Fig. 12.2.5 $I_{CCL} - T_a$

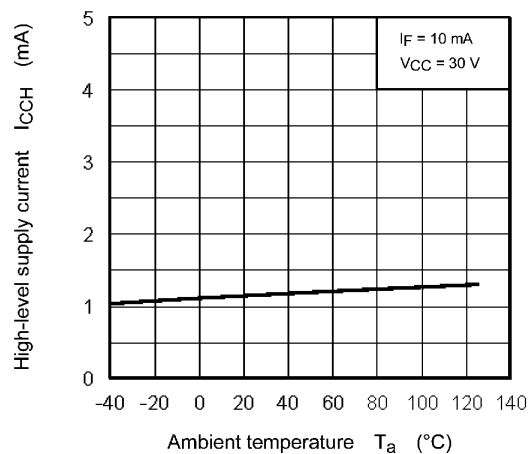


Fig. 12.2.6 $I_{CCH} - T_a$

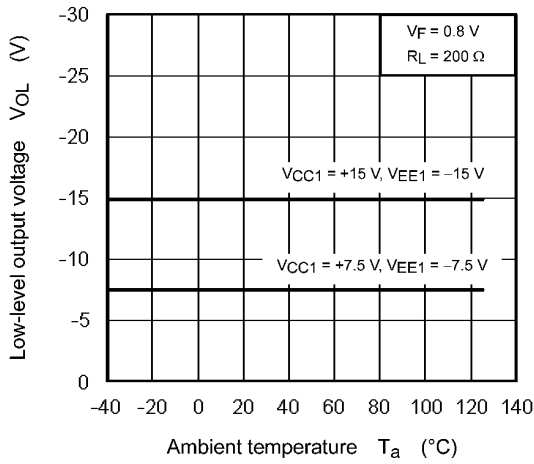


Fig. 12.2.7 $V_{OL} - T_a$

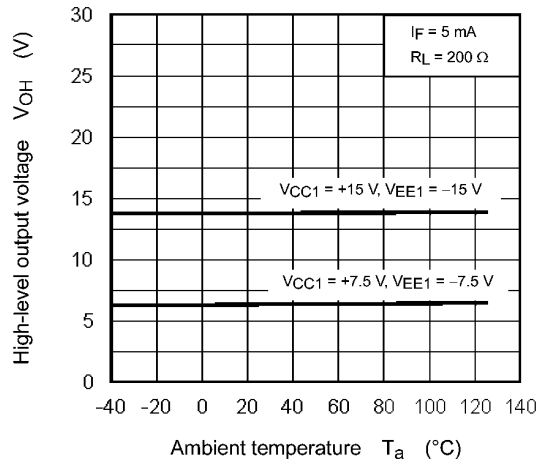


Fig. 12.2.8 $V_{OH} - T_a$

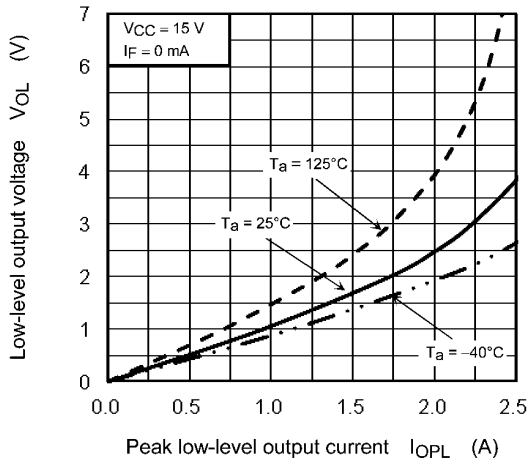


Fig. 12.2.9 $V_{OL} - I_{OLP}$

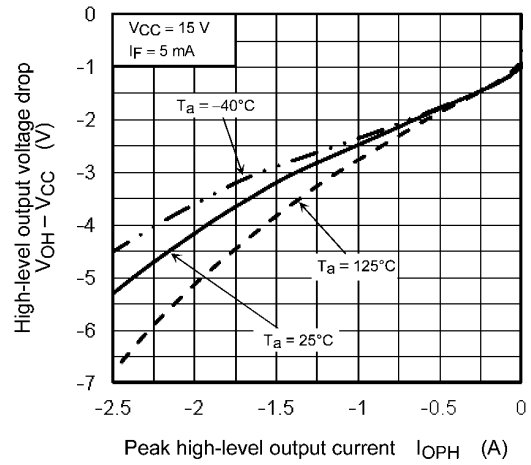


Fig. 12.2.10 $(V_{OH} - V_{CC}) - I_{OPH}$

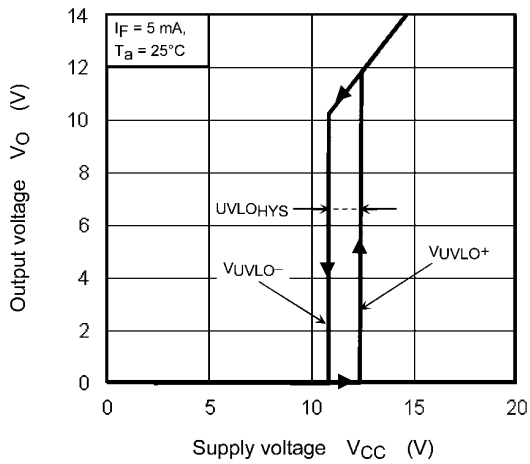


Fig. 12.2.11 $V_O(V_{UVLO}) - V_{CC}$

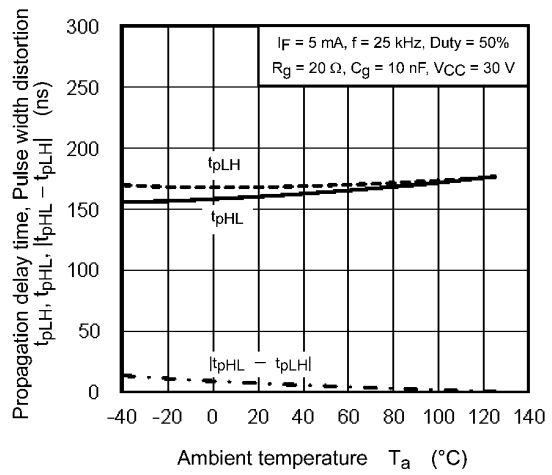


Fig. 12.2.12 $t_{pLH}, t_{pHL}, |t_{pHL} - t_{pLH}| - T_a$

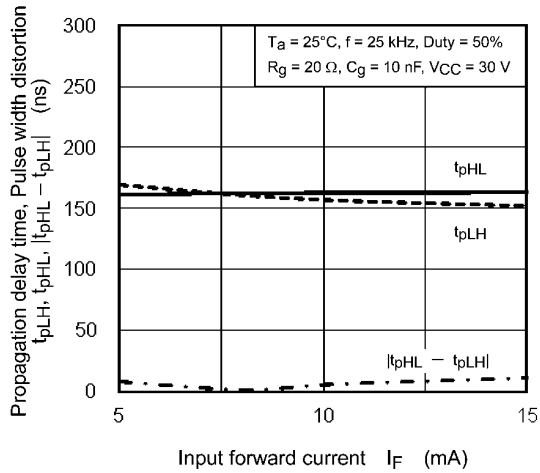


Fig. 12.2.13 $t_{pLH}, t_{pHL}, |t_{pHL} - t_{pLH}| - I_F$

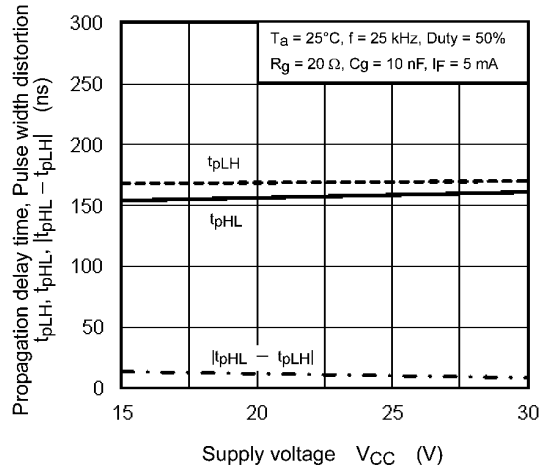


Fig. 12.2.14 $t_{pLH}, t_{pHL}, |t_{pHL} - t_{pLH}| - V_{CC}$

NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

13. Soldering and Storage

13.1. Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

- When using soldering reflow (See Fig. 13.1.1 and 13.1.2)

Reflow soldering must be performed once or twice.

The mounting should be completed with the interval from the first to the last mountings being 2 weeks.

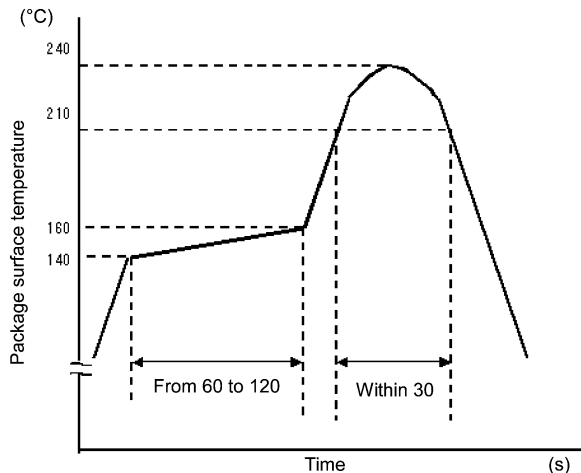


Fig. 13.1.1 An example of a temperature profile when Sn-Pb eutectic solder is used

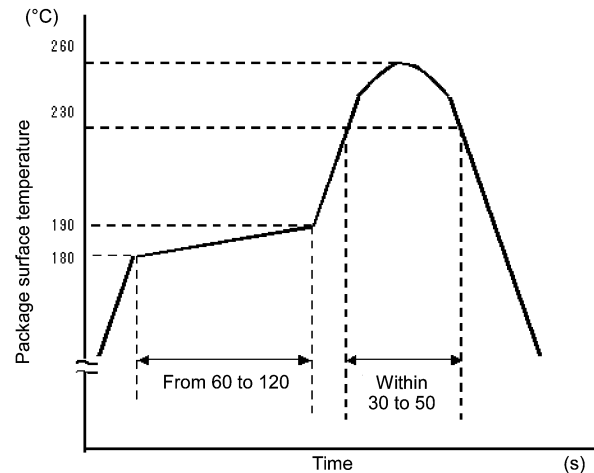


Fig. 13.1.2 An example of a temperature profile when lead(Pb)-free solder is used

- When using soldering flow (Applicable to both eutectic solder and Lead(Pb)-Free solder)
Apply preheating of 150°C for 60 to 120 seconds.
Mounting condition of 260°C within 10 seconds is recommended.
Flow soldering must be performed once.
- When using soldering Iron (Applicable to both eutectic solder and Lead(Pb)-Free solder)
Complete soldering within 10 seconds for lead temperature not exceeding 260°C or within 3 seconds not exceeding 350°C
Heating by soldering iron must be done only once per lead.

13.2. Precautions for General Storage

- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5°C to 35°C and 45% to 75%, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

14. Marking

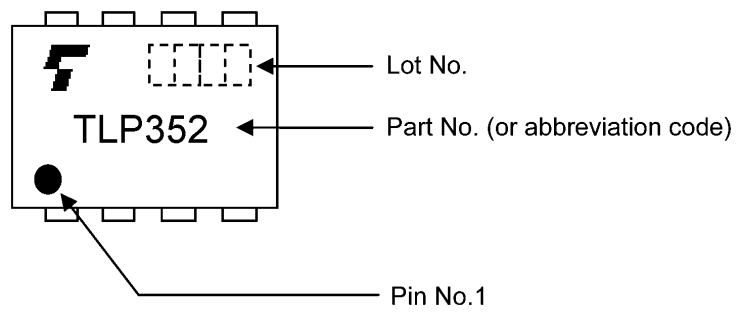
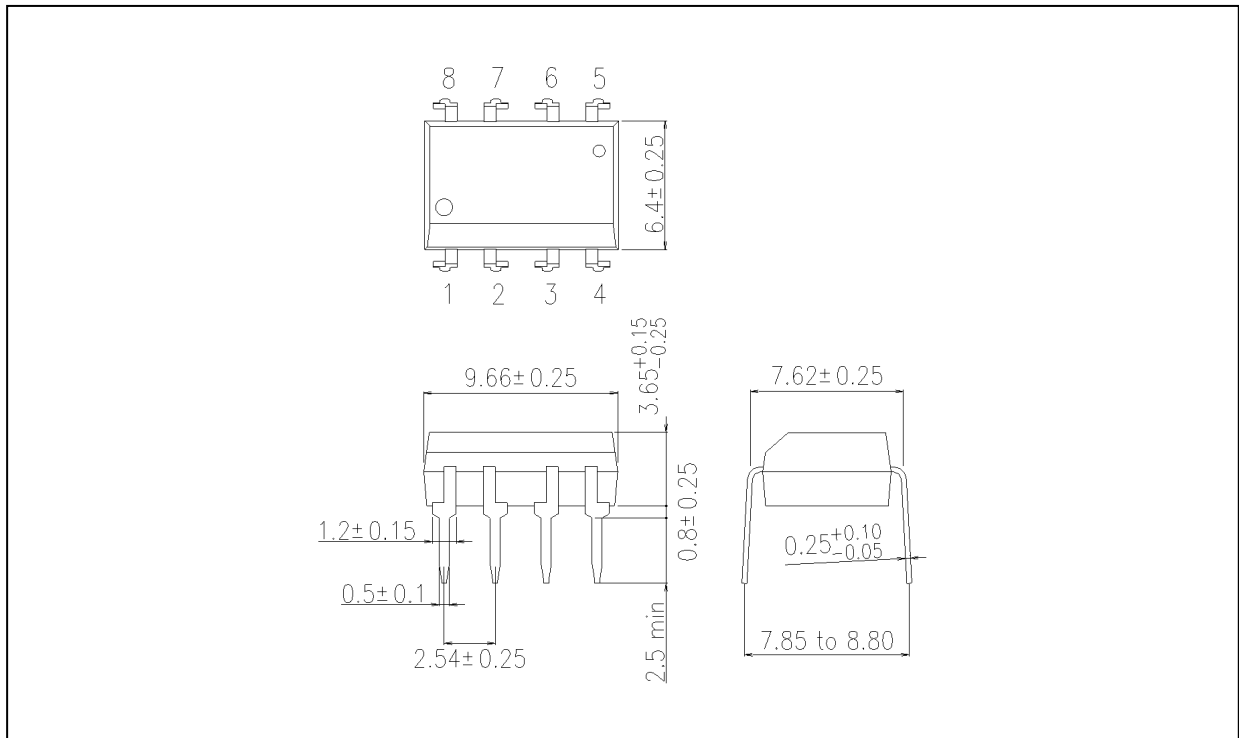


Fig. 14.1 Marking

Package Dimensions

Unit: mm



Weight: 0.54 g (typ.)

| Package Name(s) |
|-------------------|
| TOSHIBA: 11-10C4S |

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