

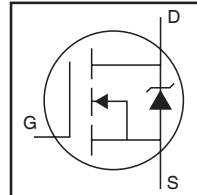
**Applications**

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

**Benefits**

- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode  $dV/dt$  and  $dI/dt$  Capability

HEXFET® Power MOSFET



$V_{DSS}$		<b>75V</b>
$R_{DS(on)}$	typ.	<b>5.0mΩ</b>
	max.	<b>6.3mΩ</b>
$I_D$		<b>130A</b>



**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	130①	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	91①	
$I_{DM}$	Pulsed Drain Current ②	510	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	250	W
	Linear Derating Factor	1.6	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$dv/dt$	Peak Diode Recovery ④	11	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ③	270	mJ
$I_{AR}$	Avalanche Current ①	See Fig. 14, 15, 16a, 16b	A
$E_{AR}$	Repetitive Avalanche Energy ⑤		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	0.61	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface , TO-220	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, TO-220 ⑥	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) , D²Pak ⑥ ⑦	—	40	

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	75	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.069	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA <sup>②</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	5.0	6.3	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 75A <sup>③</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 150μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 75V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 75V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -20V
R <sub>G</sub>	Gate Input Resistance	—	1.5	—	Ω	f = 1MHz, open drain

**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	98	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 75A
Q <sub>g</sub>	Total Gate Charge	—	120	180	nC	I <sub>D</sub> = 75A
Q <sub>gs</sub>	Gate-to-Source Charge	—	35	—		V <sub>DS</sub> = 60V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	46	—		V <sub>GS</sub> = 10V <sup>⑤</sup>
t <sub>d(on)</sub>	Turn-On Delay Time	—	26	—	ns	V <sub>DD</sub> = 48V
t <sub>r</sub>	Rise Time	—	120	—		I <sub>D</sub> = 75A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	51	—		R <sub>G</sub> = 3.9Ω
t <sub>f</sub>	Fall Time	—	63	—		V <sub>GS</sub> = 10V <sup>⑤</sup>
C <sub>iss</sub>	Input Capacitance	—	5150	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	460	—		V <sub>DS</sub> = 50V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	250	—		f = 1.0MHz
C <sub>oss</sub> eff. (ER)	Effective Output Capacitance (Energy Related)	—	570	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 60V <sup>⑦</sup> , See Fig. 11
C <sub>oss</sub> eff. (TR)	Effective Output Capacitance (Time Related) <sup>⑧</sup>	—	700	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 60V <sup>⑥</sup> , See Fig. 5

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	130 <sup>④</sup>	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>②</sup>	—	—	510	A	
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 75A, V <sub>GS</sub> = 0V <sup>⑤</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	38	57	ns	T <sub>J</sub> = 25°C V <sub>R</sub> = 64V, T <sub>J</sub> = 125°C I <sub>F</sub> = 75A
Q <sub>rr</sub>	Reverse Recovery Charge	—	65	98	nC	T <sub>J</sub> = 25°C di/dt = 100A/μs <sup>⑤</sup> T <sub>J</sub> = 125°C
I <sub>RRM</sub>	Reverse Recovery Current	—	2.8	—	A	T <sub>J</sub> = 25°C
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.096mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 75A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ④ I<sub>SD</sub> ≤ 75A, di/dt ≤ 530A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑥ C<sub>oss</sub> eff. (TR) is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ C<sub>oss</sub> eff. (ER) is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.

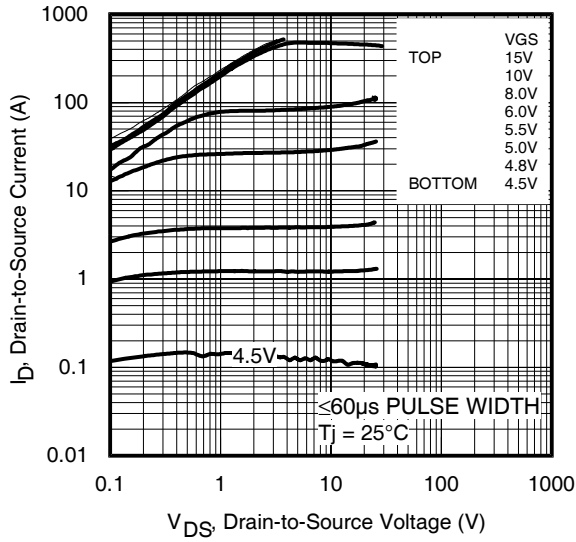


Fig 1. Typical Output Characteristics

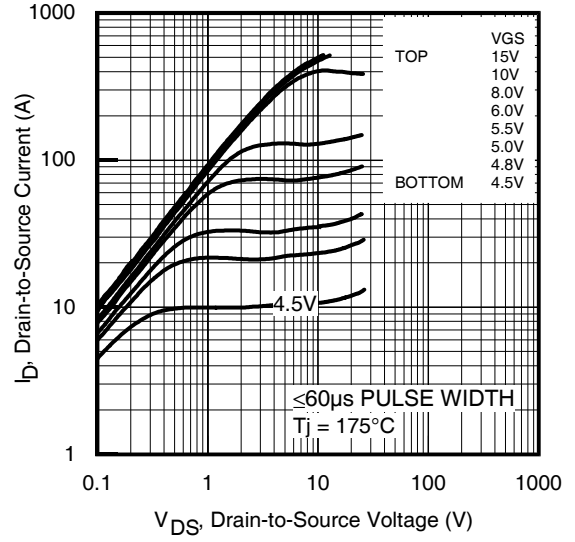


Fig 2. Typical Output Characteristics

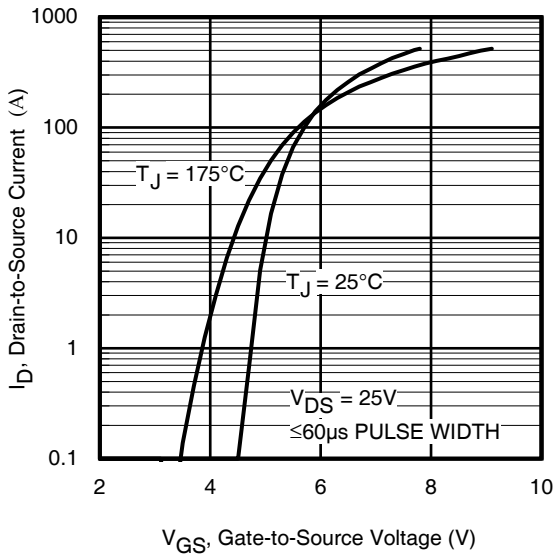


Fig 3. Typical Transfer Characteristics

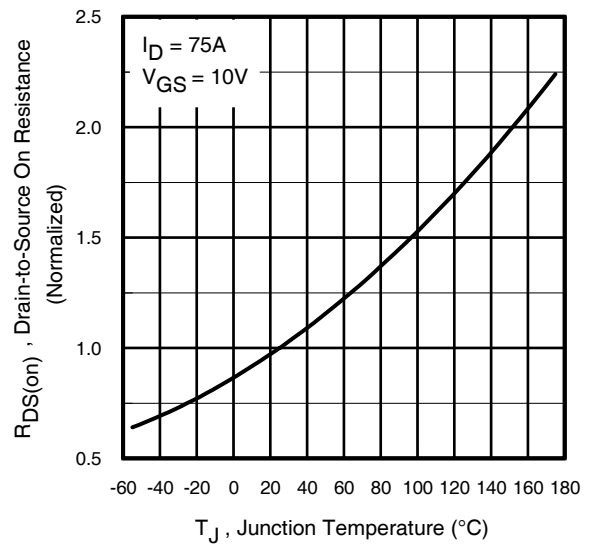


Fig 4. Normalized On-Resistance vs. Temperature

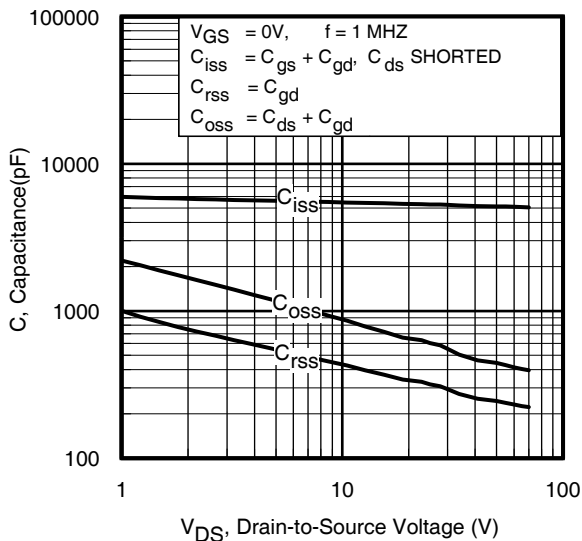


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

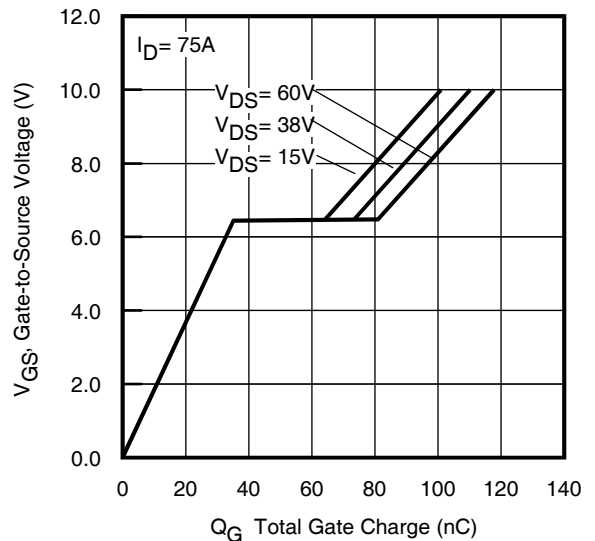


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

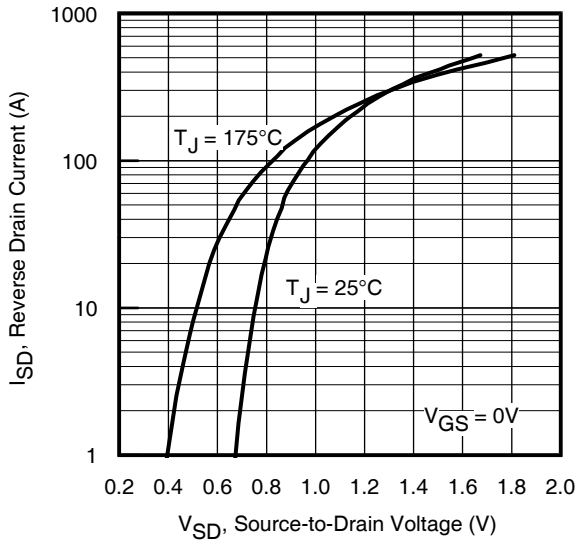


Fig 7. Typical Source-Drain Diode Forward Voltage

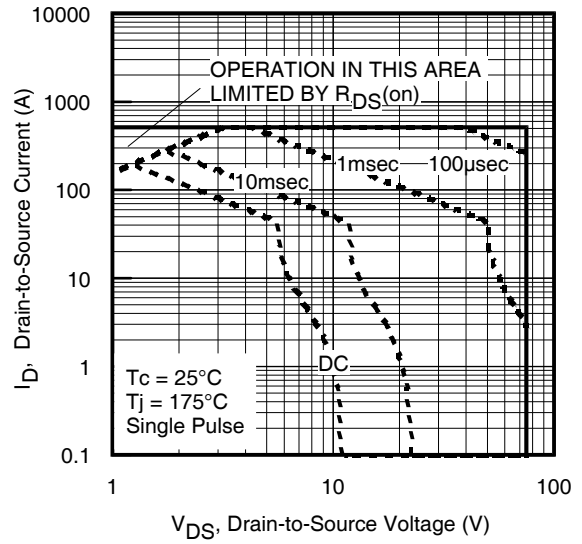


Fig 8. Maximum Safe Operating Area

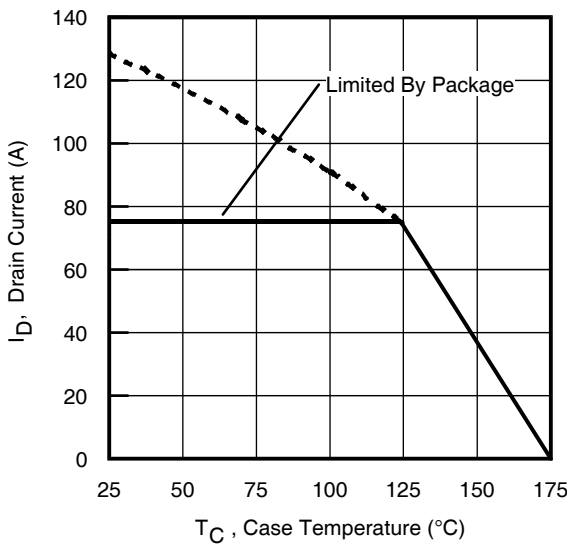


Fig 9. Maximum Drain Current vs. Case Temperature

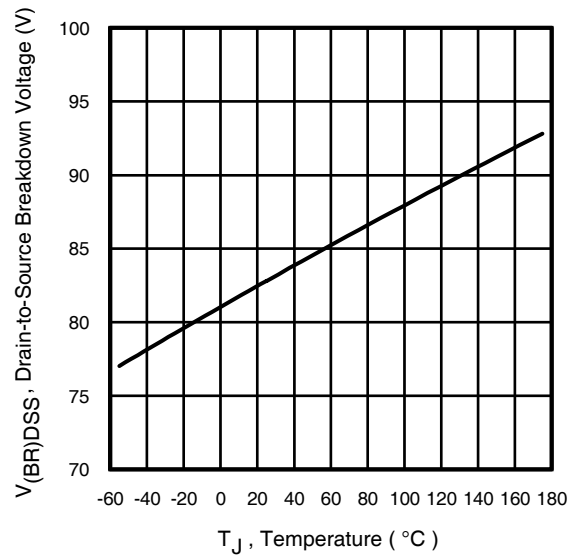


Fig 10. Drain-to-Source Breakdown Voltage

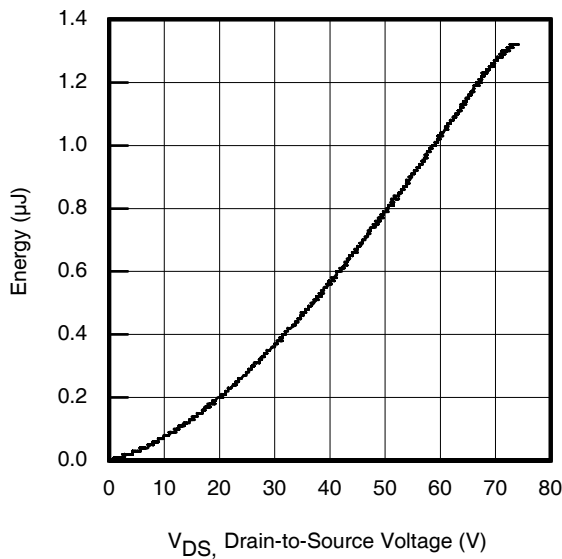


Fig 11. Typical  $C_{OSS}$  Stored Energy

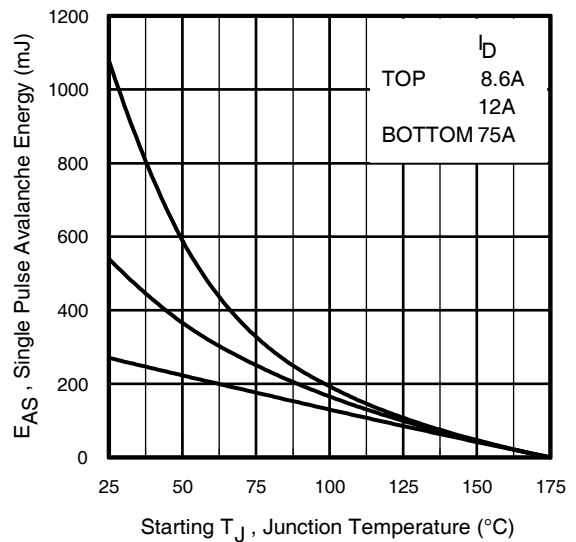


Fig 12. Maximum Avalanche Energy vs. Drain Current  
www.irf.com

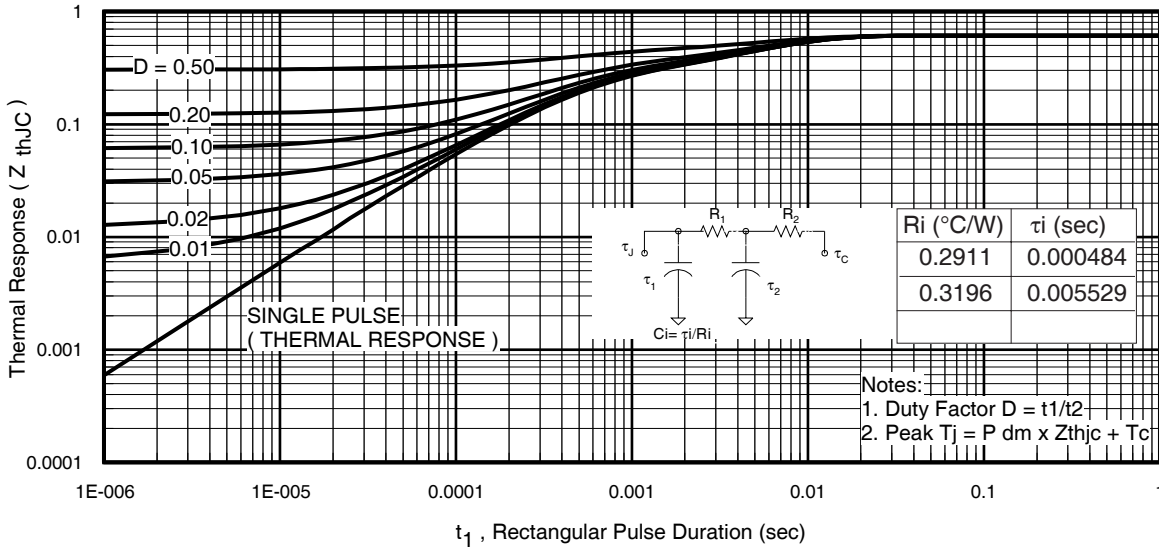


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

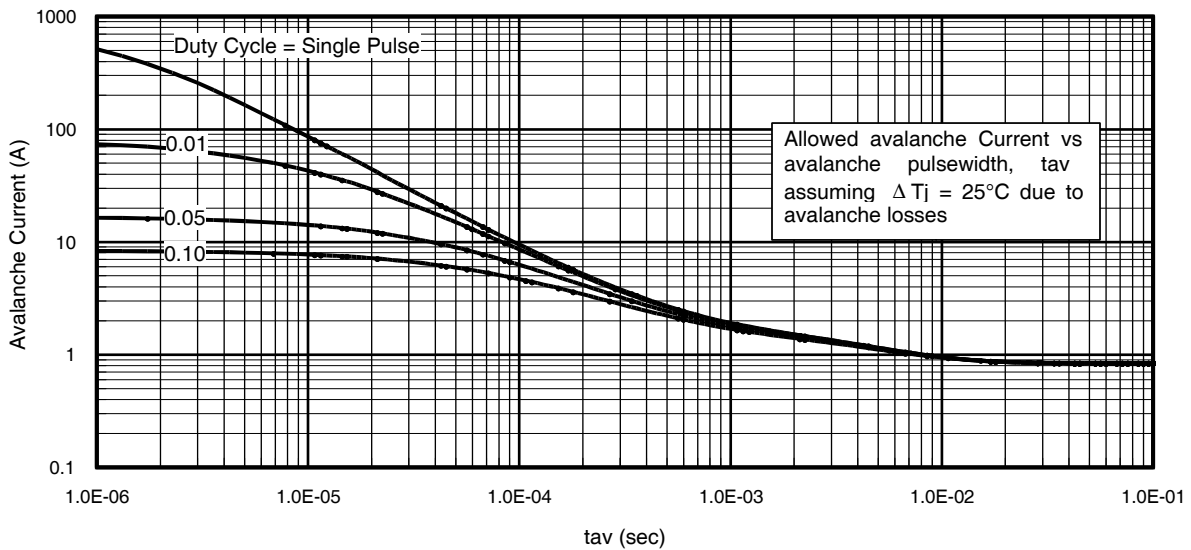
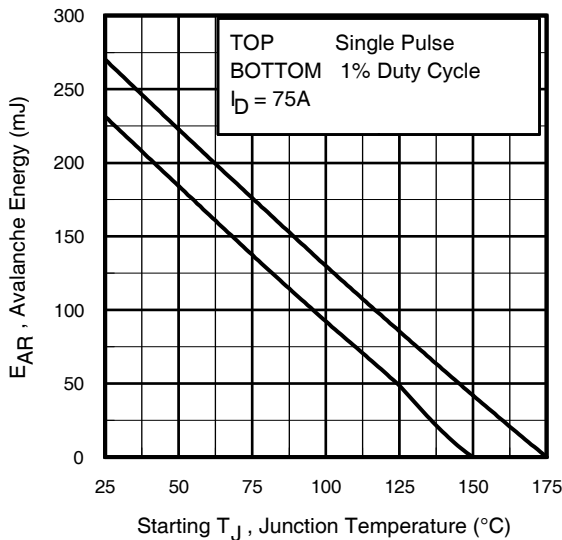


Fig 14. Typical Avalanche Current vs. Pulsewidth



**Notes on Repetitive Avalanche Curves, Figures 14, 15:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as  $25^{\circ}C$  in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

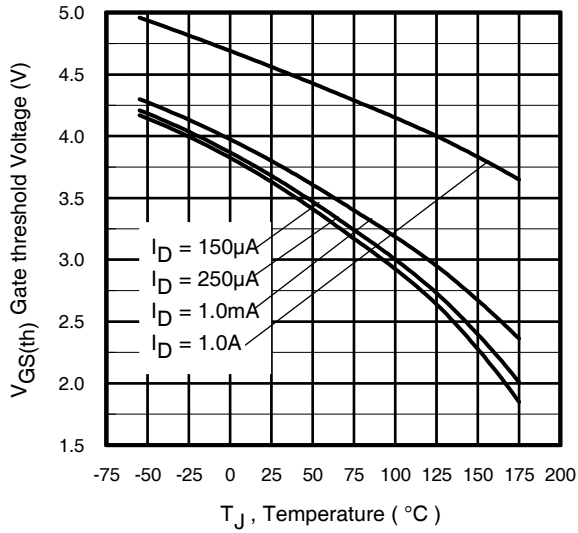


Fig 16. Threshold Voltage vs. Temperature

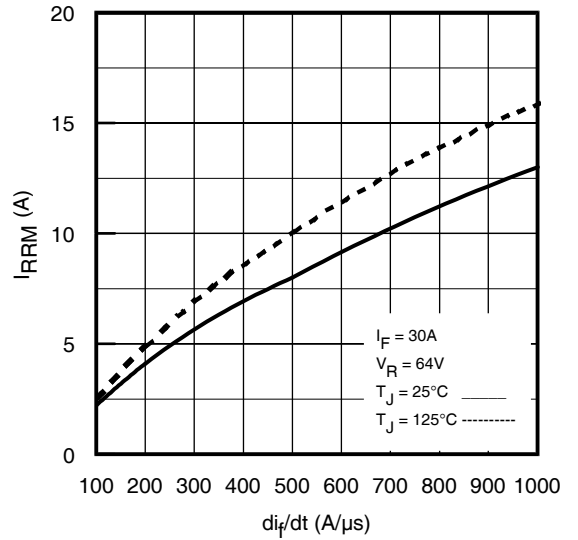


Fig. 17 - Typical Recovery Current vs.  $di/dt$

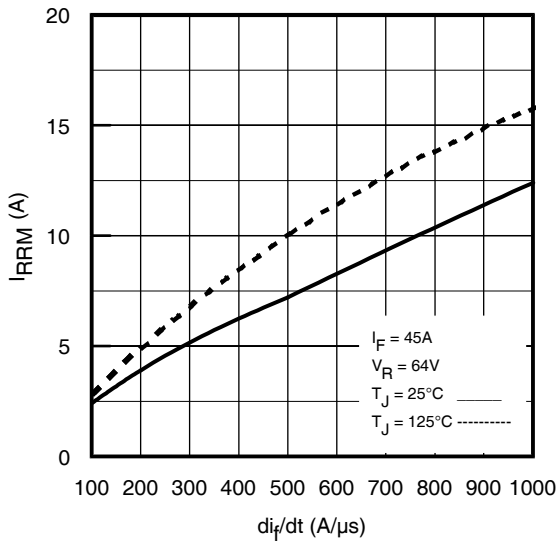


Fig. 18 - Typical Recovery Current vs.  $di/dt$

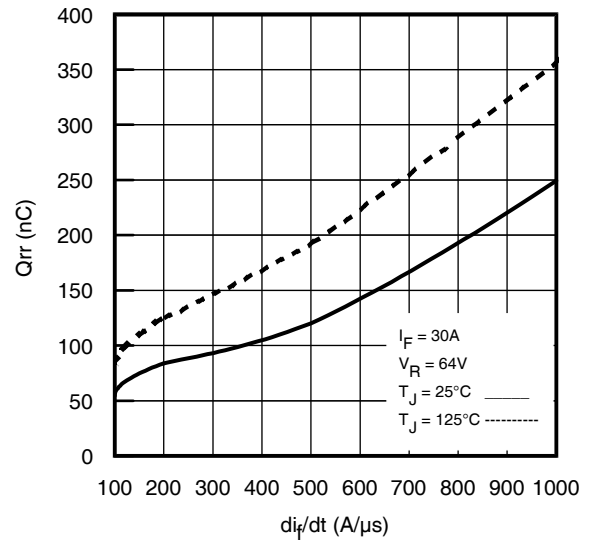


Fig. 19 - Typical Stored Charge vs.  $di/dt$

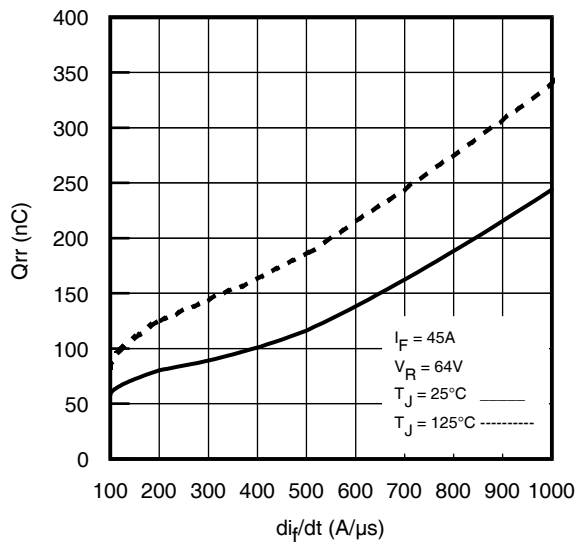
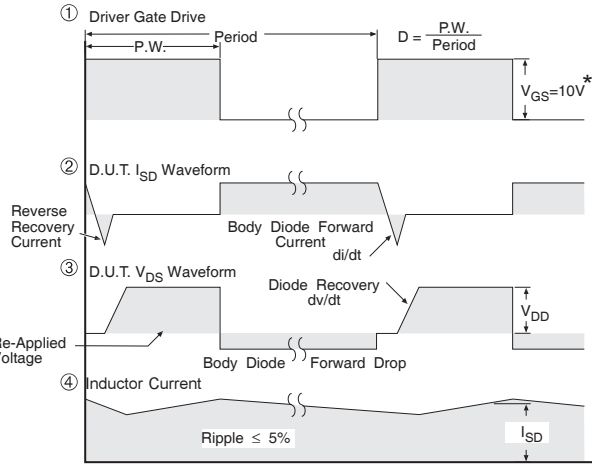
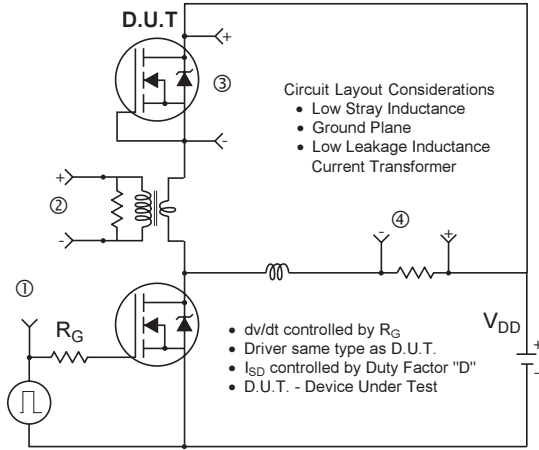
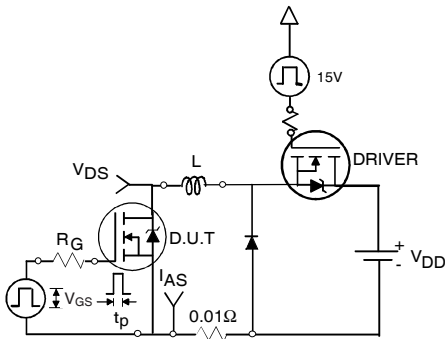


Fig. 20 - Typical Stored Charge vs.  $di/dt$

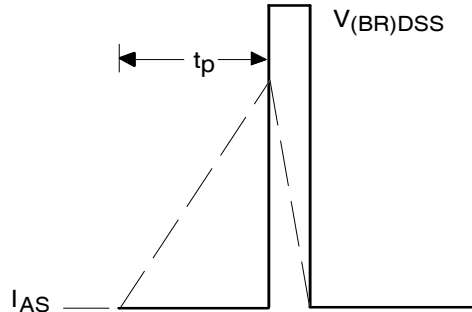


\*  $V_{GS} = 5V$  for Logic Level Devices

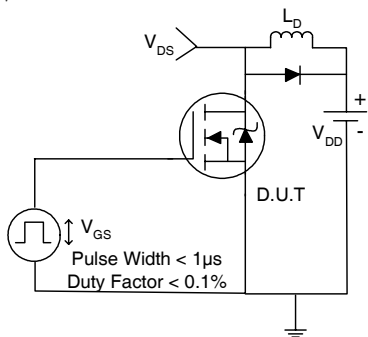
**Fig 20. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs**



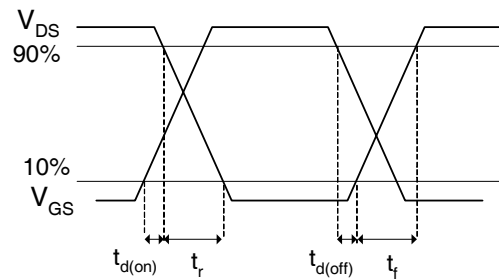
**Fig 21a. Unclamped Inductive Test Circuit**



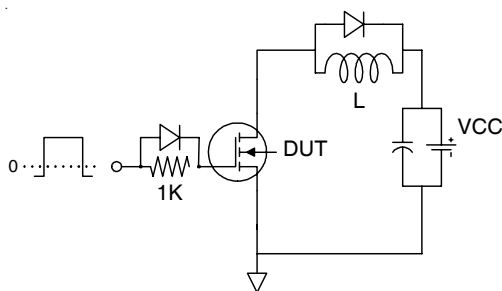
**Fig 21b. Unclamped Inductive Waveforms**



**Fig 22a. Switching Time Test Circuit**



**Fig 22b. Switching Time Waveforms**



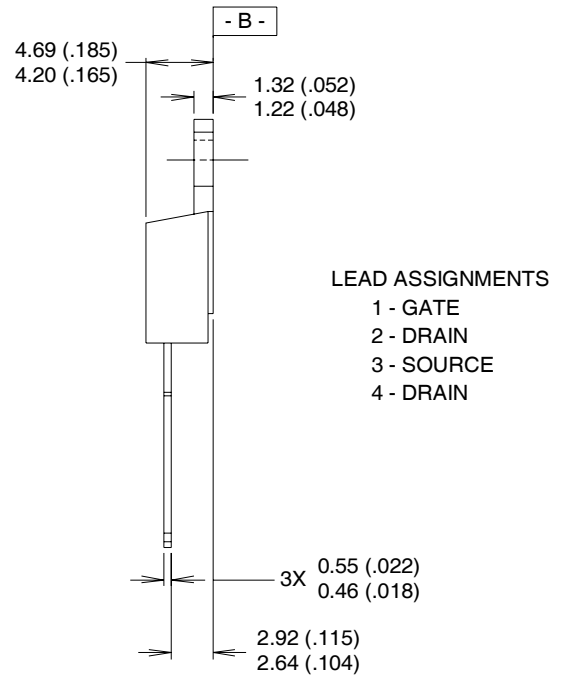
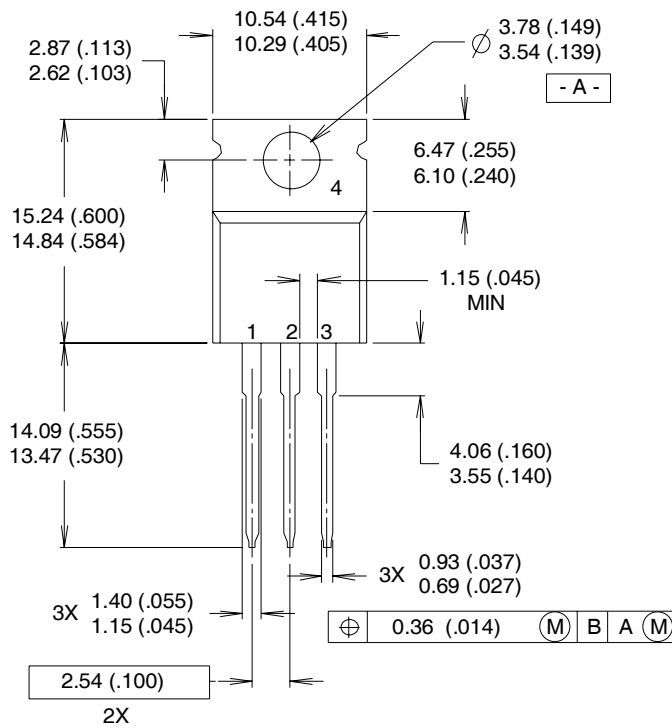
**Fig 23a. Gate Charge Test Circuit**



**Fig 23b. Gate Charge Waveform**

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



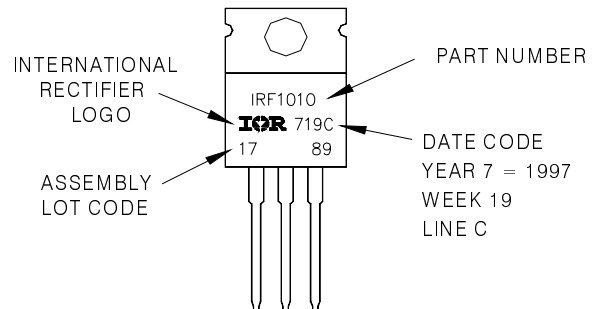
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

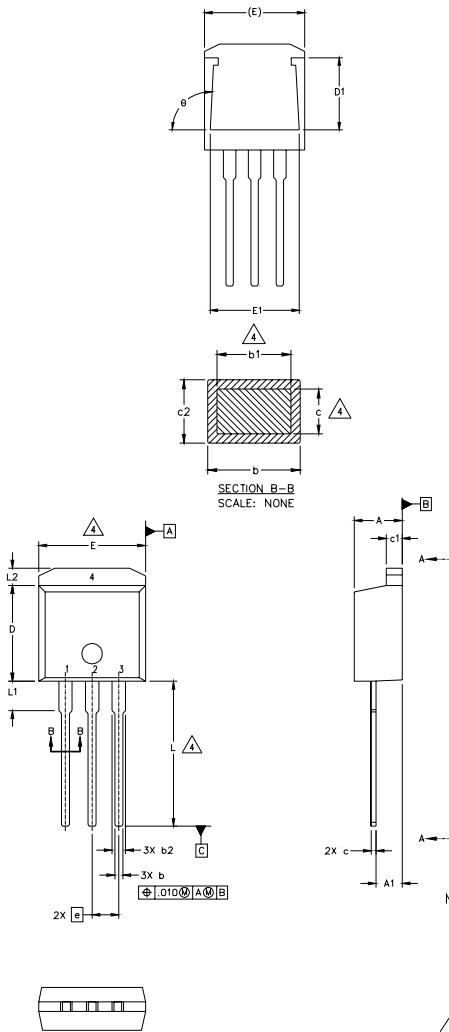
EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
**Note:** "P" in assembly line  
 position indicates "Lead-Free"



TO-220AB packages are not recommended for Surface Mount Application.



TO-262 Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190	4	
A1	2.03	2.92	.080	.115		
b	0.51	0.99	.020	.039		
b1	0.51	0.89	.020	.035		
b2	1.14	1.40	.045	.055		
c	0.38	0.63	.015	.025		4
c1	1.14	1.40	.045	.055		
c2	0.43	.063	.017	.029		3
D	8.51	9.65	.335	.380		
D1	5.33		.210			
E	9.65	10.67	.380	.420	3	
E1	6.22		.245			
e	2.54 BSC		.100 BSC			
L	13.46	14.09	.530	.555		
L1	3.56	3.71	.140	.146		
L2		1.65		.065		

LEAD ASSIGNMENTS

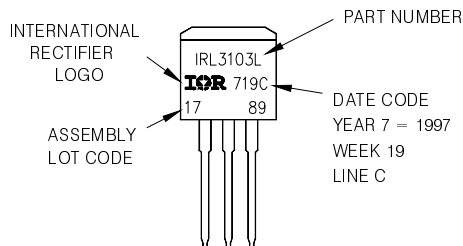
HEXFET	IGBT
1. - GATE	1- GATE
2. - DRAIN	2- COLLECTOR
3. - SOURCE	3- EMITTER
4. - DRAIN	4- COLLECTOR

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  5. CONTROLLING DIMENSION: INCH.

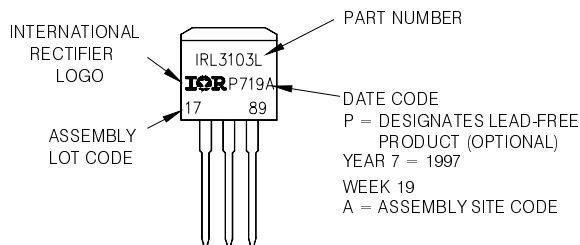
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE 'C'

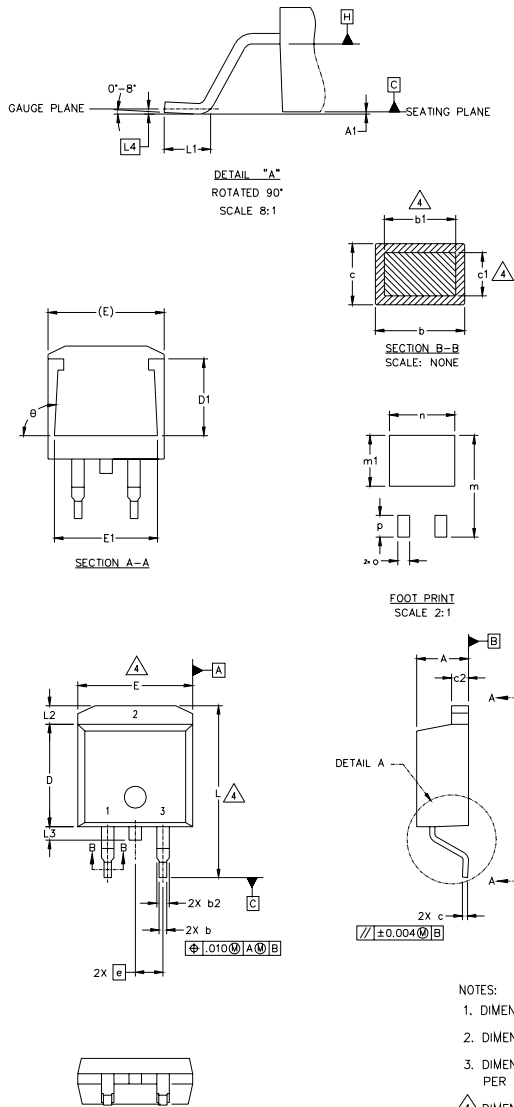
Note: 'P' in assembly line position indicates 'Lead-Free'



OR



D<sup>2</sup>Pak Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	3
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

\* PART DEPENDENT.

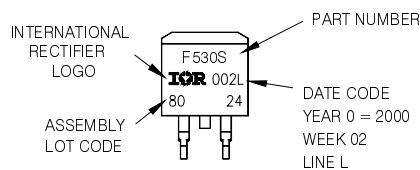
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
- CONTROLLING DIMENSION: INCH.

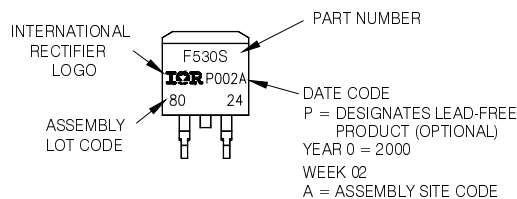
D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE 'L'

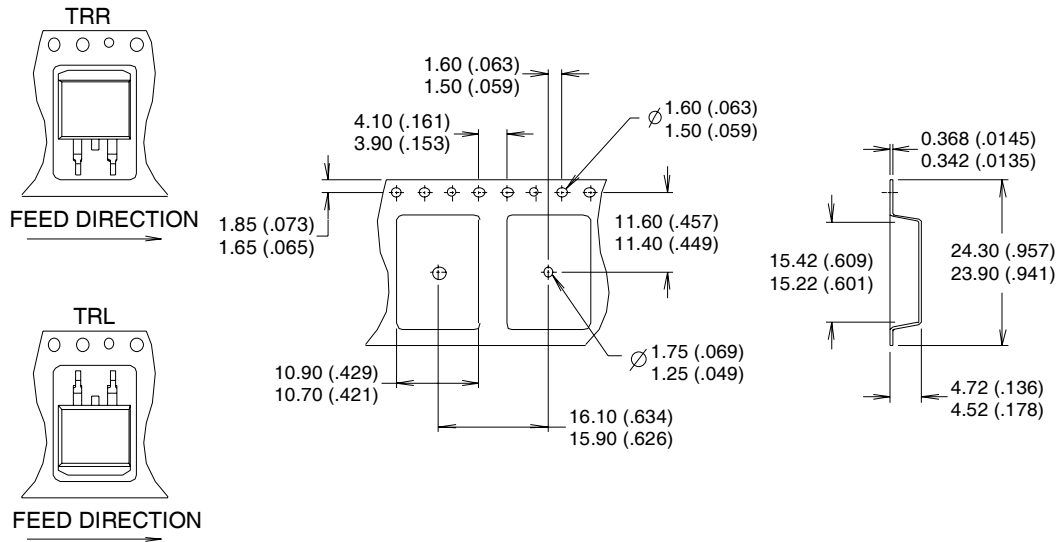
Note: 'P' in assembly line  
position indicates 'Lead-Free'



**OR**



D<sup>2</sup>Pak Tape & Reel Information



- NOTES :
1. COMFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  - ③ DIMENSION MEASURED @ HUB.
  - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Automotive [Q101] market.  
 Qualification Standards can be found on IR's Web site.